

WHAT IS CLAIMED IS:

1. A method of manufacturing a metal-oxide-semiconductor (MOS) transistor, comprising the steps of:

providing a substrate having a gate structure thereon;

5 forming a first spacer on the sidewall of the gate structure;

performing a pre-amorphization implantation to amorphize a portion of the substrate;

forming a doped source/drain extension region in the substrate on each side of the first spacer;

10 forming a second spacer on the sidewall of the first spacer;

forming a doped source/drain region in the substrate on each side of the second spacer;

performing a pre-annealing process; and

15 performing a solid phase epitaxial process to re-crystallize the amorphized portion of the substrate and activate the doped source/drain extension region and the doped source/drain region to form a source/drain terminal, wherein the annealing temperature in the pre-annealing operation is lower than the operating temperature in the solid phase epitaxial process.

2. The method of claim 1, wherein the pre-annealing process comprises placing  
20 the substrate inside a furnace and heating up the furnace.

3. The method of claim 1, wherein the pre-annealing process comprises heating to an annealing temperature between about 400°C to 500°C.

4. The method of claim 3, wherein the pre-annealing process comprises maintaining the substrate at the annealing temperature for a period of about 30 minutes.

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5. A method of manufacturing a metal-oxide-semiconductor (MOS) transistor, comprising the steps of:

providing a substrate having a gate structure thereon;

forming a first spacer on the sidewall of the gate structure;

5 performing a pre-amorphization implantation to amorphize a portion of the substrate;

forming a doped source/drain extension region in the substrate on each side of the first spacer;

forming a second spacer on the sidewall of the first spacer;

10 forming a doped source/drain region in the substrate on each side of the second spacer;

performing a solid phase epitaxial process to re-crystallize the amorphized portion of the substrate and activate the doped source/drain extension region and the doped source/drain region to form a source/drain terminal, wherein the annealing

15 temperature in the pre-annealing operation is lower than the operating temperature in the solid phase epitaxial process; and

performing a post-annealing process, wherein the annealing temperature in the post-annealing operation is higher than the operating temperature in the solid phase epitaxial process.

20 6. The method of claim 5, wherein the post-annealing operation comprises performing a rapid thermal annealing process.

7. The method of claim 5, wherein the post-annealing process comprises heating the substrate to an annealing temperature of about 850°C.

8. The method of claim 7, wherein the post-annealing process comprises maintaining the substrate at the annealing temperature for a period of about 20 seconds.

9. The method of claim 5, wherein the post-annealing process comprises heating the substrate to an annealing temperature between about 900°C to 1000°C.

5        10. The method of claim 9, wherein the post-annealing process comprises maintaining the substrate at the annealing temperature for a spike period.

11. A method of manufacturing a metal-oxide-semiconductor (MOS) transistor, comprising the steps of:

providing a substrate having a gate structure thereon;

10        forming a first spacer on the sidewall of the gate structure;

performing a pre-amorphization implantation to amorphize a portion of the substrate;

forming a doped source/drain extension region in the substrate on each side of the first spacer;

15        forming a second spacer on the sidewall of the first spacer;

forming a doped source/drain region in the substrate on each side of the second spacer;

performing a pre-annealing process;

performing a solid phase epitaxial process to re-crystallize the amorphized  
20    portion of the substrate and activate the doped source/drain extension region and the doped source/drain region to form a source/drain terminal, wherein the annealing temperature in the pre-annealing operation is lower than the operating temperature in the solid phase epitaxial process; and

performing a post-annealing process, wherein the annealing temperature in the post-annealing operation is higher than the operating temperature in the solid phase epitaxial process.

12. The method of claim 11, wherein the pre-annealing process comprises placing  
5 the substrate inside a furnace and heating up the furnace.

13. The method of claim 11, wherein the pre-annealing process comprises heating to an annealing temperature between about 400°C to 500°C.

14. The method of claim 13, wherein the pre-annealing process comprises maintaining the substrate at the annealing temperature for a period of about 30 minutes.

10 15. The method of claim 11, wherein the post-annealing operation comprises performing a rapid thermal annealing process.

16. The method of claim 11, wherein the post-annealing process comprises heating the substrate to an annealing temperature of about 850°C.

17. The method of claim 16, wherein the post-annealing process comprises  
15 maintaining the substrate at the annealing temperature for a period of about 20 seconds.

18. The method of claim 11, wherein the post-annealing process comprises heating the substrate to an annealing temperature between about 900°C to 1000°C.

19. The method of claim 18, wherein the post-annealing process comprises maintaining the substrate at the annealing temperature for a spike period.